REMARKS

Applicant respectfully requests reconsideration and allowance of the subject application in view of the amendments and the remarks to follow. Claims 32, 38, 42 and 45 have been amended, claim 7 has been canceled and new claims 46-53 have been added. Claims 1-6 and 8-53 are pending in this application.

The amendments to the specification and drawings address minor informalities noted during review and bring the specification and drawings into mutual conformance. More specifically, the amendments to Fig. 3 merely correct reference numbers and eliminate inadvertent reference number duplication, and the amendment to page 12 corrects a minor grammatical error. No new matter is added by the amendments to the specification and drawing.

The Examiner's approval of the amendments to Fig. 3 is respectfully requested. Revised formal drawing is enclosed under separate cover addressed to the Chief Draftsperson.

New claims 46-53 are supported at least by text appearing at page 4, line 14 through page 15, line 17 of the application as originally filed. New claims 46 et seq. are similar to claim 1 et seq. but differ in scope. No new matter is added by new claims 46 et seq. New claims 46 et seq. distinguish over the art of record and are allowable.

Objections to the Claims:

Claims 6 and 7 are stated (p. 2, item 1) to be objected to as being substantial duplicates of one another. Claim 7 has been canceled in response to the concerns noted in the Office Action.

35 U.S.C. § 112

Claims 32, 38, 42 and 45 are stated to be rejected under 35 U.S.C. 112, 2ND as being indefinite. While the grounds for rejection are unclear to Applicant, in the spirit of cooperation and in order to advance the prosecution of the application, claims 32, 38, 42 and 45 have been amended to place them in independent form and to attempt to address the cognitive dissonance discussed in the Office Action, however, these amendments are not intended to alter the scope of the claims.

The Office Action states (p. 3, item 3) that "Where applicant acts as his or her own lexicographer ...." The Office Action states that the term "exposes" in claims 2, 20, 30 and 41 is used to mean "contains", and that the accepted meaning is "shows" and then states that Applicant's usage gives rise to indefiniteness in those claims. Applicant finds this puzzling at least in part because the Office Action does not state that such claims are rejected on indefiniteness grounds. Clarification is requested.

Further, the interpretation of the usage of the term "exposes" postulated in the Office Action (p. 3) is incomprehensible to Applicant. These claims respectively recite:

"the file system exposes a set of application program interfaces that are used by an application" (claim 2);

"An operating system for an integrated circuit (IC) module, comprising: a file system to manage access to data files stored in both volatile memory and nonvolatile memory; and an application program interface (API) to expose the file system to applications" (claim 20);

"exposing functions to manipulate the data files, the same functions being used regardless of whether the data files are located on the volatile memory or the nonvolatile memory" (claim 30); and

"exposing a common set of functions to manipulate both the volatile data files and the nonvolatile data files" (claim 41).

Such is described in the specification at least at p. 5, line 18 et seq. Applicant is unable to envision how the definition or interpretation contained in the Office Action could possibly comport with the subject matter recited in these claims. Clarification is requested.

Put another way, the interpretation provided in the Office Action appears to give the term "exposes" a meaning repugnant to the ordinary meaning of the term. Such is improper, as is explained below in more detail with reference to MPEP §2111.01, entitled "Plain Meaning". This MPEP section states that "THE WORDS OF A CLAIM MUST BE GIVEN THEIR "PLAIN MEANING" UNLESS THEY ARE DEFINED IN THE SPECIFICATION". Such is also explained in more detail as noted below:

> While the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allow. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) (discussed

> below). One must bear in mind that, especially in nonchemical cases, the words in a claim are generally not limited in their meaning by what is shown or disclosed in the specification. It is only when the specification provides definitions for terms appearing in the claims that the specification can be used in interpreting claim language. *In re Vogel*, 422 F.2d 438, 441, 164 USPQ 619, 622 (CCPA 1970).

Thus, for at least these reasons, Applicant respectfully submits that claims 32, 38, 42 and 45, as presented and as amended, comply with 35 U.S.C. §112, and that claims 2, 20, 30 and 41 also comply with such statute. As such, any rejections or objections on indefiniteness grounds should be withdrawn. Applicant respectfully notes that claims 2, 20, 30, 32, 38, 41, 42 and 45 comply with 35 U.S.C. §112, and that claims 2, 20, 30, 32, 38, 41, 42 and 45 should be allowed.

35 U.S.C. § 102

Claim 1 stands rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,421,279 B1 to Tobita et al. (hereinafter "Tobita"). The Office Action also presents argument (p. 3, item 6) indicative that the Examiner contemplates rejection of claim 8 as being anticipated. Applicant respectfully disagrees and requests reconsideration.

Anticipation is a legal term of art. Applicant notes that in order to provide a valid finding of anticipation, several conditions must be met: (i) the reference must include every element of the claim within the four corners of the reference (see MPEP §2121); (ii) the elements must be set forth as they are recited in the claim (see MPEP §2131); (iii) the teachings of the reference cannot be modified (see MPEP §706.02, stating that "No question of obviousness is present" in conjunction with anticipation); and (iv) the reference must enable the invention as recited in the claim (see MPEP §2121.01). Additionally, (v) these conditions must be simultaneously satisfied.

Tobita is directed (see, e.g., Title) to a "flash memory control method and apparatus processing system therewith". Tobita teaches (see Abstract) that "A semiconductor file system features a first nonvolatile memory electrically erasable, a second nonvolatile memory not electrically erasable, a volatile memory, a controller, and a control section which controls the controller wherein a physical address corresponding to a logical address specified from an external system is accessed. The first nonvolatile memory stores data for the external system to perform operations, first management information indicating correspondence between physical and logical addresses, and second management

information indicating a state of the first nonvolatile memory. The second nonvolatile memory previously stores interface information. The controller determines a physical sector address. The control section is for controlling input/output of data from/to the external system and for temporarily storing write data into the first nonvolatile memory from the external system in the volatile memory and then transferring the write data from the volatile memory to the first nonvolatile memory."

In contrast, claim 1 recites "An integrated circuit (IC) module comprising: a processor; volatile memory and nonvolatile memory operatively coupled to the processor; and a file system to manage access to one or more data files stored in the volatile memory and in the nonvolatile memory", which is not taught or disclosed by Tobita.

The Office Action cites (pp. 3, 4) diverse portions of Tobita as providing the various elements described with reference to claim 1. Applicant notes that Tobita describes a number of different embodiments (see, e.g., Brief Description, col. 14, line 5 though col. 18, line 12, with reference to 103 Figures). More specifically, Figs. 1-48 are explicitly stated to relate to a first embodiment, Figs. 50-60 are explicitly stated to relate to a second embodiment, Figs. 61-81 are explicitly stated to relate to a third embodiment and Figs. 49 and 82-103 are explicitly stated to relate to a fourth ("forth") embodiment. Within this context, Tobita provides numerous different alternative examples or sub-embodiments.

It is inappropriate to combine elements "picked and chosen" from diverse embodiments in attempting to arrive at a finding of anticipation. In part, this is because a finding of anticipation involves determining that the subject matter

recited in the claim is already in the public domain, using the rules of evidence set forth in the statute and which are further interpreted in the MPEP and case law. In order to provide evidence of anticipation, the reference must, within its four corners, set forth this subject matter (item (ii) supra) and enable (item (iv) supra) exactly as it appears in the claim.

In other words, selecting elements from diverse portions of the reference comprises impermissible modification of (e.g., addition to) the teachings of the reference (i.e., see item (iii) supra). Further, because none of items (ii)-(iv) needed in order to provide a valid finding of anticipation are met, item (v) cannot be met. The rejection of claim 1 fails at least four necessary criteria needed in order to determine that the subject matter of the claim is anticipated. This is explained below in more detail.

The Office Action cites:

col. 47 (p. 3), corresponding to the fourth embodiment, as providing a processor (see, e.g., col. 45, line 64 and col. 46, line 50);

cols. 4 and 47 (p. 4), corresponding to the Summary and the fourth embodiment, respectively, as providing a volatile and a non-volatile memory coupled to the processor;

cols. 4 and 31, corresponding respectively to the Summary and the second embodiment (see col. 31, line 30); and

cols. 45 and 46, corresponding to the fourth embodiment.

Furthermore, the teachings of the reference are misinterpreted in the Office Action. For example, the Office Action states (p. 4) that col. 4, lines 24-25 describe "... volatile memory and non-volatile memory operatively coupled to the

processor". Col. 4, lines 24 and 25 states that: "Whether the main memory is volatile or non-volatile makes a great difference".

The Office Action further states (p. 4) that col. 47, lines 26-29 teaches this aspect of the claimed subject matter. Col. 47, lines 26-29 states that: "Numeral 4015 is a ROM which stores a control program and numeral 4016 is a processor which executes the control program for controlling the entire information processing system of the invention." Neither of these passages provides the elements for which they are cited.

The Office Action additionally states (p. 4) that "... and a file system to manage access to one or more data files..." is taught at col. 4, lines 58-60. Col. 4, lines 58-60 states that: "It is therefore an object of the invention to provide a file system using a high-performance and inexpensive flash memory as the storage medium." This passage is completely void of any mention of data files or any system to manage access to any files.

The Office Action also states (p. 4) that this aspect of the claimed subject matter is taught at col. 31, lines 32-54. This passage is directed to Embodiment 2 (line 29) and the following paragraph, which includes the cited portion, states that:

> A second embodiment of the invention is described. FIG. 50 is a block diagram of the second embodiment of the invention. A flash memory system according to the second embodiment of the invention comprises a flash memory 2001 as storage media, a bus 2002 of an information apparatus used as a host of the flash memory system, an interface circuit 2003 consisting of registers, buses, etc., for interfacing with the host bus 2002, a controller (control section) 2004 which controls the entire flash memory system, an address translation table (information storage means) 2005 for converting from logical addresses used for the host to manage file data into physical addresses indicating physical storage locations, a write buffer 2006 for storing at high speed file data transferred from the host to raise apparent processing speed (therefore, volatile memory such as SRAM or DRAM meeting the demand for high-speed

> writing), a DMA (dynamic memory access) controller 2007 for overcoming the weak point that the operation speed of the controller 2004 is lower than that of the host bus 2002 to transfer data at high speed, and an interrupt information register (interrupt information storage means) 2008 for storing the operation state when processing is interrupted upon receipt of an access request from the host while data in the write buffer 2006 is being transferred to the flash memory 2001. (The operation state is stored for later restart.)

"File data", as referenced in this passage, are data describing a file. Data files are files of data relating to some aspect or thing other than the data file itself. The two concepts are not the same and are not arbitrarily interchangeable.

For yet further example, the Office Action cites (p. 4) col. 45, lines 66-67 and col. 46, lines 1-8 as teaching "... stored in the volatile memory and the non-volatile memory ...", where the first ellipsis corresponds to "a file system to manage access to one or more data files", as recited in claim 1.

This passage states that: "FIG. 82 is a block diagram of an information processing system according to the fourth embodiment of the invention, wherein numeral 4001 is a CPU (central processing unit) which executes programs and processes data, numeral 4002 is a flash memory which is a large-capacity nonvolatile memory storing the programs, data, etc., handled by the CPU 4001, and numeral 4003 is a cache memory which is a volatile memory temporarily storing data such as data transferred from the flash memory and write data from the CPU 4001." This passage is void of any teaching of "a file system to manage access to one or more data files stored in the volatile memory and the non-volatile memory", as recited in claim 1, and the Office Action provides no indication that such is found in Tobita.

As such, the rejection of claim 1 also fails to meet the criteria set forth in item (i) supra. Accordingly, the anticipation rejection of claim 1 is prima facie defective and should be withdrawn, and claim 1 should be allowed.

Claim 8 recites "An integrated circuit (IC) module as recited in claim 1, further comprising at least one application stored in the nonvolatile memory and executable on the processor to request access to the one or more data files", which is not taught or disclosed by Tobita.

The Office Action cites col. 6, lines 52-55 as teaching this aspect of the claimed subject matter. Col. 6, lines 52-55 states that: "If all the above-mentioned points are implemented, the three types of memory can cover various applications and the number of parts can be reduced compared with installation of a memory for each application." "Application", as employed in this passage, does not refer to any "application ... executable by the processor" or to such that is executable "to request access to the one or more data files" as recited in claim 8. It is a reference to a field of deployment for the overall system, for example, information processing (col. 1, lines 20-22; in conjunction with miniaturized IC cards, col. 6, line 56).

The Office Action also cites col. 45, line 66 through col. 46, line 8 as providing teaching of this affirmatively-recited aspect of the subject matter of claim 8. This passage, which is reproduced above with reference to claim 1, is void of any mention of the word "application" and as such cannot possibly provide the subject matter for which it is cited.

The Office Action cites (p. 4) col. 19, lines 65 through col. 20, line 3 as providing "... and executable on the processor ...", as recited in claim 8, where the

first ellipsis corresponds to "at least one application stored in the nonvolatile memory ..." and the second ellipsis corresponds to "to request access to the one or more data files", also as recited in claim 8.

Col. 19, line 65 through col. 20, line 3 refers to the first embodiment (col. 18, line 19) and thus this passage is disjoint from the other portions cited in conjunction with rejection of claim 8 and accordingly is inapposite thereto with respect to anticipation. Further, the paragraph extending from col. 19, line 63 to col. 20, line 10, which includes this passage, states that:

> The operation of the semiconductor file system according to the embodiment is discussed. First, sector transfer is described. The sector transfer includes a sector write for executing sector transfer from the host to a write buffer in PSRAM, a sector read for executing sector transfer from PSRAM, FLASH, and MASK ROM to the host, multitransfer for executing the sector transfer a plurality of times, and long transfer with ECC data. The sector transfer mode is selected by the microcomputer which analyzes a command written into a command register (not shown) contained in the register section 1046 shown in FIG. 5 and writes the transfer mode into a sector transfer control register 1692 shown in FIG. 8. After the transfer mode is set in the sector transfer start register 1691 by the microcomputer, the sector transfer is started as triggered from the host.

This passage provides no teaching or disclosure of the subject matter which it is cited as representing. Clarification is requested.

The anticipation rejection of claim 8 thus also fails all five prongs of the tests noted above. As a result, the anticipation rejection of claim 8 is clearly prima facie defective and should be withdrawn, and claim 8 should be allowed.

35 U.S.C. § 103

Claims 2-45 stand variously rejected under 35 U.S.C. §103(a) as being unpatentable over one or more of Tobita, U.S. Patent No. 6,519,594 B1 to Li (hereinafter "Li"), U.S. Patent No. 6,542,955 B1 to Chen (hereinafter "Chen"), U.S. Patent No. 6,587,873 B1 to Nobakht et al. (hereinafter "Nobakht"). Claim 7 has been canceled, rendering rejection of such moot. Applicant respectfully disagrees and requests reconsideration.

In responding to such a rejection, it is helpful to first review the subject matter addressed by the references. Tobita has been at least partially discussed above with reference to the response to the anticipation rejection.

Li describes "computer-implemented sharing of java classes for increased memory efficiency and communication method" (Title). More specifically, Li states (Abstract) that:

> A computer-implemented method and system for allowing Java classes to be shared among many Java virtual machines (JVMs) including a communication system allowing Java and native applications to readily interoperate. An implementation of the JVM on an operating system platform, e.g., the Aperios AV/OS, allows a variety of applications including desktop applications, applets and Internet based applications, home networking applications, MHEG-6 applets, gaming, gaming applications and next generation audio visual applications to operate with the operating system. The present invention provides a shared memory pool (SMP) into which a JVM and store and register a particular Java class. The stored and registered Java class is then accessible by other JVMs using the SMP and a Java layer class manager that is implemented in software. The Java layer class manager requires other JVMs to access a key for the stored class in order to synchronize access to the Java class among several installed and operating JVMs of the computer system. By sharing common Java classes in this fashion, the memory resource overhead required to operate multiple JVMs on a common computer system is drastically reduced thereby allowing a multiple JVM platform to be operable on an embedded computer system. A novel communication method is also disclosed for communicating information between a JVM application and a native application

using the computer system's operating system. The novel communication method also allows multiple JVM applications to communicate using the shared memory pool. These functions are incorporated into a JavaLayer that supports the full PersonalJava™ platform.

Chen describes a "microcontroller virtual memory system and method" (Title). More specifically, Chen states (Abstract) that:

> A microcontroller memory system that provides on-chip, non-volatile memory for internal data and program code storage in such a manner that all on-chip, non-volatile memory is efficiently utilized. In one embodiment, a microcontroller memory scheme allows internal program code and data stored in the non-volatile memory to be reprogrammed in place by software executing on the microcontroller or by external devices through the microcontroller's serial port. In another embodiment, data and program code stored in the internal program area can be accessed using any instruction employed to access via an internal data bus the contents of an on-chip, volatile memory. The non-volatile memory used to store the program code and internal data can be implemented with Flash memory or EEPROM. To enable compatibility with conventional 8051 controllers, a flag in a special function register is provided that indicates whether a memory access is to be into the non-volatile memory or, in the conventional manner, into internal volatile or external volatile memory used for data (as opposed to program) storage.

Nobakht describes a "system server for channel-based internet network" (Title). More specifically, Nobakht states (Abstract) that:

> A system server for a channel-based network including one or more Internet sites and one or more user terminals. The system server includes a channel table database storing a master channel table that includes a list of channel numbers, each channel number having an associated Internet address and an associated Internet site name. Each Internet site of the network is addressable by an associated Internet address stored in the master channel table. The system server includes a network database and an update manager database. The system server identifies each user terminal requesting service by comparing transmitted identification information with authorized user information stored in the network database. The system server also compares a channel table version number from the requesting user terminal with a version number stored in the update manager database that is associated with the master channel table, and notifies each requesting user terminal when updated channel table information is available. At each user terminal, a user reads the

channel numbers and associated Internet site names from a menu displaying the downloaded channel table, selects an Internet site name from the displayed menu, and enters the channel number associated with the selected Internet site name using an input device that is similar to a television remote control.

In contrast, independent claim 10 recites: "An integrated circuit (IC) module comprising: a processor; volatile memory operatively coupled to the processor, the volatile memory storing volatile data in at least one data file; nonvolatile memory operatively coupled to the processor, the nonvolatile memory storing nonvolatile data in at least one data file; a memory region directory to identify whether a requested data file is located in the volatile memory or in the nonvolatile memory; and a file location specifier to specify a physical location of the requested data file within the volatile memory or the nonvolatile memory identified by the memory region directory as containing the requested data file", which is not taught, disclosed, suggested or motivated by the cited references, alone or in any proper combination.

The Office Action states (p. 8) that col. 4, lines 24-25 describes "... volatile memory operatively coupled to the processor ..." and that such passage also describes "... non-volatile memory operatively coupled to the processor ...." Col. 4, lines 24 and 25 states that: "Whether the main memory is volatile or non-volatile makes a great difference". This passage makes no mention whatsoever of coupling volatile or nonvolatile memory to a processor, and certainly does not even suggest or motivate the combination recited in claim 10.

The Office Action states (p. 8) that "... a memory region directory ..." is found in Tobita at col. 38, lines 19-38. First, claim 10 recites "a memory region directory to identify whether a requested data file is located in the volatile memory or in the nonvolatile memory", which is not what is cited in the Office Action.

Second, the cited portion of Tobita discusses allocation of different portions 3108 and 3109 of a flash memory 3126, i.e., a non-volatile read write memory (see, e.g., col. 36, line 48 et seq., element 3106, line 64 et seq., Fig. 62). This passage thus describes management of multiple sections of a non-volatile memory.

Third, Tobita only employs the term "directory" four times (col. 2, lines 6, 9, 13 and 47), and then only to describe shortfalls in prior art systems. As such, Tobita does not teach usage of directories for memory management.

Fourth, Tobita teaches (col. 2, line 3 et seq.) that directories and FATs can cause problems because they are more frequently written to than other portions of storage media when this type of organization is employed with flash memories. Tobita states (col. 2, line 3 et seq.) that:

> The limit of the write count mentioned above will introduce a serious problem with the use of the flash memory as storage media of a semiconductor disk. For example, data is written into areas such as a directory and FAT (file allocation table) on a disk more frequently than other areas, that is, data is frequently written into only specific blocks of the flash memory allocated to the directory and FAT and there is a good chance that the write count limit of the flash memory will be exceeded in the specific blocks faster than in other blocks. If the write count limit is exceeded, the elements are degraded and it may be impossible to carry out a normal read or write. If a directory or FAT on a disk is destroyed, the entire disk cannot be read. Therefore, malfunction only in specific blocks makes the entire semiconductor disk unusable, leading to poor efficiency.

As such, Tobita teaches away from use of memory directories. It is improper to employ a reference in a combination when the reference teaches away from the combination. This is explained more fully in MPEP 2145(X)(D)(2), entitled "References Cannot Be Combined Where Reference Teaches Away from Their Combination". This MPEP section states that: "It is improper to combine references where the references teach away from their combination. *In re*

Grasselli, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983)". In this instance, because the reference is being employed to arrive at the subject matter of the claim and because the reference teaches away from that subject matter, the reference cannot be properly employed to attempt to find unpatentability.

The Office Action states (p. 9) that "Chen teaches identifying whether data is in volatile or non-volatile memory as follows:

"... to identify whether a requested data file is located in the volatile memory or in the nonvolatile memory ..." at col. 6, lines 16-19." However, this is not what is recited in claim 10. Claim 10 recites "... a memory region directory to identify whether a requested data file is located in the volatile memory or in the nonvolatile memory ...."

The cited portion of Chen states that: "The state of the NVMEN flag 242 determines whether a data memory access is into the non-volatile memory 220' or volatile memory (e.g., into of the internal data SRAM 230, SFR 240 or external data SRAM 212)." A flag is typically a single bit. Chen teaches two states, SET and CLEARED, for this flag, and states (col. 8, lines 55-58) that: "In the programming mode, the NVMEN bit is set and the MOVX (or other appropriate instructions) can be used for reconfiguring the internal program code." and that (col. 6, lines 13-15): "In one embodiment, the NVMEN flag 242 is a single bit in the SFR 240 that can be set by either external or internal programs." A single bit cannot be employed to realize a memory region directory, as affirmatively recited in claim 10. Accordingly, the combination proposed in the Office Action does not provide the subject matter of claim 10.

Further, the Office Action cites diverse portions of Tobita (p. 8, item 14) as corresponding to various affirmatively-recited aspects of the subject matter of claim 10 and states (p. 9) that "Tobita does not teach identifying whether data is in volatile or non-volatile memory". The Office Action then states (p. 9, item 15) that Chen provides such teaching. The Office Action then offers the naked conclusion that "It would have been obvious ...." but fails to identify any motivation in either reference to modify and/or combine teachings.

There is no teaching or guidance identified within Tobita to aid one of ordinary skill in picking and choosing elements from the diverse embodiments of Tobita or in assembling those elements to attempt to arrive at the subject matter of any of Applicant's claims. As such, the rejection employs an improper "obvious to try" standard of unpatentability.

Such is improper, as is discussed below in more detail with reference to MPEP §2145(X)(B), entitled "Obvious To Try Rationale". This MPEP section states that "The admonition that 'obvious to try' is not the standard under §103 has been directed mainly at two kinds of error. In some cases, what would have been 'obvious to try' would have been to vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful. In others, what was 'obvious to try' was to explore a new technology or general approach that seemed to be a promising field of experimentation, where the prior art gave only general guidance as to the particular form of the claimed invention or how to achieve it."

In re O'Farrell, 853 F.2d 894, 903, 7 USPQ2d 1673, 1681 (Fed. Cir. 1988) (citations omitted)".

In this instance, no guidance in selecting some but not others of the many elements from the many embodiments of Tobita is identified. Similarly, no direction as to which of many possible choices is likely to be successful has been identified.

As there is no basis for the Examiner's contentions within the cited references, the only possible motivation for these contentions is hindsight reconstruction wherein the Examiner is utilizing Applicant's own disclosure to construct a reason for combining and/or modifying the teachings of the cited references. The Examiner is reminded that hindsight reconstruction is not an appropriate basis for a §103 rejection. (See, e.g., *Interconnect Planning Corp. v. Feil*, 227 USPQ 543, 551 (Fed. Cir. 1985); *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990) (explaining that hindsight reconstruction is an improper basis for rejection of a claim).)

Additionally, independent claim 18 recites: "A file system for an integrated circuit module, comprising: means for handling a request for a data file stored on the integrated circuit module; means for identifying whether the data file is located in volatile memory or nonvolatile memory; and means for specifying a physical location of the data file within the volatile memory or the nonvolatile memory", which is not taught, disclosed, suggested or motivated by the cited references, alone or in combination.

The Office Action cites (p. 9) Tobita, col. 6, lines 20-22 and col. 7, lines 30-34 as providing "... means for handling the request for a data file stored on the

integrated circuit module ...." Col. 6, lines 20-22 of Tobita states that: "The nonvolatile memory not electrically erasable is used as a memory to store interface information, such as the IC card internal configuration and access format." Such cannot possibly substitute for this affirmatively-recited element.

Col. 7, lines 30-34 of Tobita states that: "The data stored in the buffer memory is transferred to the flash memory when the external system, such as the host system, does not make an access request, that is, when the flash memory system waits for the external system to make an access request." This passage is unrelated to handling any request for stored data files and instead relates to storage of data.

The Office Action cites (p. 9) col. 6, lines 16-19 of Chen with respect to "means for identifying whether the data file is located in volatile memory or nonvolatile memory". The NVMEN flag 240 taught by Chen is used (col. 6, line 3 et seq.) to determine whether to access an internal SRAM 234 or SFR 240 or a non-volatile memory 220. It has no particular relationship to any data file (see, e.g., Table 1) and may be set by either internal or external programs (see line 14). As a result, the proposed combination does not provide the elements recited in claim 18.

Further, independent claim 20 recites "An operating system for an integrated circuit (IC) module, comprising: a file system to manage access to data files stored in both volatile memory and nonvolatile memory; and an application program interface (API) to expose the file system to applications", which is not taught, disclosed, suggested or motivated by the cited references, alone or in combination.

The portions (col. 4, lines 58-60 and col. 31, lines 32-54) of Tobita cited in the Office Action (p. 14, item 29) as providing "... a file system to manage access to data files ...." are explicitly stated to use a flash memory, i.e., a nonvolatile memory, as a storage medium. The latter passage describes temporary use of SRAM as a write buffer 2006 to aid in the speed with which files can be transferred from a host to flash memory and does not describe a file system as recited in claim 20.

The portion (col. 45, line 66 through col. 46, line 8) of Tobita cited (p. 15) in the Office Action as providing "... stored in both volatile memory and nonvolatile memory ..." refers (see col. 45, line 64 et seq.) to a fourth embodiment again involving use of RAM for temporarily storing (see col. 46, line 6) data as a step towards storage of the data in nonvolatile memory for subsequent access.

The portions (col. 4, lines 58-60 and col. 6, lines 52-55) of Tobita cited (p. 15) in the Office Action as corresponding to "... to expose the file system to applications ..." respectively refer to flash memory and multiple memories but are void of any mention of anything discernibly related to "an application program interface (API) to expose the file system to applications", as recited in claim 20. The passing mention of "application" in col. 6 refers to a field of deployment for the system and does not refer to an application program.

The Office Action cites (p. 15) Li at col. 6, lines 31-37 as providing an application program interface. The application program interface 125 is described in this passage exclusively in the context of nonvolatile memories (device module 135, Fig. 3, listing mini disk, hard disc, flash ROM, CD ROM, tape). As a result,

the proposed combination does not and cannot render unpatentable the subject matter recited in claim 20.

Moreover, independent claim 25 recites "A file system for an integrated circuit module, comprising: an application program interface to enable an application to access files stored in volatile memory and nonvolatile memory; and a memory region directory to identify whether a file is stored in the volatile memory or the nonvolatile memory", which is not taught, disclosed, suggested or motivated by the cited references, alone or in combination.

The portions of Tobita cited (p. 17) as providing "... to access files stored in volatile memory and nonvolatile memory ..." are discussed above with reference to claim 20. The portion (col. 38, lines 19-38) of Tobita cited (p. 17) as providing "... and a memory region directory ..." is directed to tables 3205 and 3206 for storing address information relative to a flash (nonvolatile) memory 3106 divided into portions such as 3108 and 3109 (see col. 37, line 38 et seq.) and are unrelated to "a memory region directory to identify whether a file is stored in the volatile memory or the nonvolatile memory", as recited in claim 25. The passage referenced (p. 17, Office Action) in Li (col. 6, lines 31-38) is discussed above with reference to claim 20. Accordingly, claim 25 is patentable over the proposed combination of references.

Yet further, independent claim 28 recites "A computer-readable medium storing computer-executable instructions that, when executed on a smart card, direct the smart card to: store data in a volatile data file within volatile memory of the smart card; and facilitate access to the volatile data file by one or more

applications", which is not taught, disclosed, suggested or motivated by the cited references, alone or in combination.

The Office Action cites (p. 20) Tobita at col. 6, lines 52-54 and col. 7, lines 30-34 as providing "... and facilitate access to the volatile data file by one or more applications ...". As noted above with reference to claim 20, the passing mention of "application" in col. 6 is a reference to a field of deployment and not to a software application executing on a processor. As noted above with reference to claim 18, the passage in col. 7 is unrelated to handling any request for stored data files and instead relates to storage of data.

The Office Action cites (p. 20) col. 5, lines 47-55 of Li as providing "... store data in a volatile data file within volatile memory ..."

The cited portion of Li is reproduced below:

> In general, computer system 112 of FIG. 2 includes an address/data bus 100 for communicating information, a central processor 101 coupled with the bus for processing information and instructions, a volatile memory 102 (e.g., random access memory RAM) coupled with the bus 100 for storing information and instructions for the central processor 101 and a non-volatile memory 103 (e.g., read only memory ROM) coupled with the bus 100 for storing static information and instructions for the processor 101. Computer system 112 also includes a data storage device 104 ("disk subsystem") such as a magnetic or optical disk and disk drive coupled with the bus 100 for storing information and instructions and a display device 105 coupled to the bus 100 for displaying information to the computer user. System 112 can also be referred to as an embedded system.

In other words, this portion of Li describes a conventional computer system such as a personal computer. In such systems, the volatile memory is used to temporarily store information relative to a specific application, and respective portions of the nonvolatile and volatile memories are set aside for data storage.

The portions of the volatile memory that are set aside for use by a particular application are exclusively dedicated to that application. At various times, the application may write data files to the nonvolatile memory. As a result, the application generates requests to access the information that is stored in the various portions of memory, but it does not receive requests for data that would ordinarily be stored in either volatile or nonvolatile memory.

One reason that volatile memory regions are exclusively apportioned, i.e., are not used for storage of data files that may be accessed by a request such as recited in claim 39, is that when one application overwrites data in volatile memory regions that have been dedicated for exclusive use by another application, the data that had been stored by the another application are lost. Often, when this happens, the new data are so grossly incommensurate with the data formats employed by the another application that, when those data are accessed the another application, the another application "crashes".

When an application accidentally overwrites ("bombs") data stored in volatile memory areas employed by at least some operating system portions, and those volatile memory areas are subsequently accessed by the operating system, the operating system "crashes". This often results in serious computer malfunction usually requiring a "re-boot" in which the computer re-initializes and then reallocates all volatile memory etc.

Against this backdrop, it is apparent that volatile memory in conventional computers is employed in such a manner that the term "volatile data file" is inapposite to such systems. Put another way, to "facilitate access to the volatile

data file by one or more applications" does not comport with normal or appropriate operation of computer systems such as that described by Li.

Nobakht is cited (p. 20) as providing "... of the smart card ...". However, this excerpt as provided in the Office Action fails to reflect the recitation of claim 28. Claim 28 recites "... computer-executable instructions that, when executed on a smart card, direct the smart card to: store data in a volatile data file within volatile memory of the smart card ...." Nobakht describes a conventional smart card 232 having a non-volatile memory 330 (see fig. 3B; col. 6, lines 42-49) and provides no mention of any volatile memory or volatile data files in the context of the smart card 232. Nobakht fails to provide (i) execution of computer-executable instructions (ii) that, when executed on a smart card (iii) store data in a volatile data file (iv) within a volatile memory (v) on a smart card, as recited in claim 28.

As a result, the cited references fail to provide the elements of claim 28 and the proposed combination does not reflect and cannot render unpatentable the subject matter of claim 28. Accordingly, claim 28 distinguishes over the references cited and should be allowed.

As well, independent claim 29 recites "A method for operating an integrated circuit (IC) module, comprising: receiving a request for a data file stored on the IC module; identifying, within the IC module, whether the data file is located in volatile memory or nonvolatile memory; and specifying a physical location of the data file within the volatile memory or the nonvolatile memory", which is not taught, disclosed, suggested or motivated by the cited references, alone or in combination.

The Office Action states (p. 10) that "... receiving a request for a data file stored on the IC module ..." is taught by Tobita at col. 6, lines 20-22 and col. 7, lines 3-15. Col. 6, lines 20-22 states that: "The nonvolatile memory not electrically erasable is used as a memory to store interface information, such as the IC card internal configuration and access format." This bears no apparent relationship to requests for data files.

Col. 7, lines 3-16 of Tobita states that:

> According to the invention, there is further provided a flash memory system comprising a flash memory for storing data from an external system, means for temporarily storing the data from the external system upon receipt of a request to write the data into the flash memory, and a control section which stores the data in the data storage means upon receipt of the request to write the data, then transfers the data to the flash memory, wherein upon receipt of a new request to write data into the same address from the external system before completion of transfer of the data to the flash memory, the control section interrupts the data transfer to the flash memory and stores the new data from the external system in the data storage means and invalidates the current data being transferred to the flash memory.

This passage is unrelated to handling any request for stored data files and instead relates to storage of data. These passages are non sequitur to the aspects of claim 29 for which they are cited.

The Office Action states (p. 10) that "... identifying ... whether the data file is located in volatile memory or nonvolatile memory ..." is taught by Chen at col. 6, lines 16-19. However, this is not what is recited in claim 29. Claim 29 recites "identifying, within the IC module, whether the data file is located in volatile memory or nonvolatile memory". Chen provides no discussion whatsoever of IC modules. In fact, Chen is void of the terms "IC", "module" and "integrated circuit". Further, the cited passage is discussed above with reference to claim 10.

As a result, the rejection of claim 29 is prima facie defective and should be withdrawn, and claim 29 should be allowed.

Independent claim 33 recites "A method comprising: storing data in a volatile data file in volatile memory of an integrated circuit module; receiving, from a requestor, a request to access the volatile data file on the integrated circuit module; evaluating whether the requestor is authorized to access the volatile data file; and in an event that the requestor is authorized, locating the volatile data file in the volatile memory", which is not taught, disclosed, suggested or motivated by the cited references, alone or in combination.

The Office Action cites (p. 21) Tobita at col. 6, lines 20-22; col. 45, line 66 though col. 46, line 8 with respect to claim 33. These portions of Tobita have been discussed above with reference to the rejection of claim 18 and claim 20. The Office Action also cites col. 7, lines 3-5. This passage is exclusively devoted to storage of data in flash (nonvolatile) memory. However, claim 33 recites "... storing data in a volatile data file in volatile memory ...." and thus is unrelated to that aspect of Tobita.

The Office Action also cites (p. 21) col. 31, lines 32-35 of Tobita with reference to access of a volatile data file. As noted above with respect to claim 20, col. 31, lines 32-54 of Tobita describes temporary use of SRAM as a write buffer 2006 to aid in the speed with which files can be transferred from a host to flash memory and does not describe a volatile data file or such that can be accessed. The Office Action further cites col. 45, line 66 through col. 46, line 8, previously discussed. These passages are non sequitur with respect to any volatile data file or access thereto.

The Office Action further cites (p. 21) col. 46, lines 59-66 of Tobita as providing "... locating the volatile data file in the volatile memory ...". Col. 46, line 59 et seq. states that:

> Referring again to FIG. 82, the CPU 4001 accesses the cache memory 4003 via the memory bus 4007. The access address is input to the address comparison circuit 4005, which then compares the address with addresses previously registered in the address array 4004. If the address matches one of the registered addresses, which will be hereinafter referred to as an "address hit," the controller 4006 accesses the location in the cache memory 4003 corresponding to the address. In contrast, if the address does not match any of the registered addresses, which will be hereinafter referred to as an "address miss," the controller 4006 registers the address in the address array 4004. After this, the controller 4006 transfers the data corresponding to the address to the cache memory for storage and accesses the location in the flash memory 4002 corresponding to the address.

Consonant with the above description, cache memories are not generally used to store data files and the above passage certainly does not describe or suggest such. Cache memories typically are limited-capacity but very high speed memories that are very tightly coupled to a processor. Cache memories are used to store addresses and/or data elements and/or instructions that are repeatedly demanded by the processor. Cache memories are employed for these purposes and within this operational purview because this can significantly reduce memory access time, particularly with tasks involving repetitive processor instructions or memory accessions, and thus increase overall system operation speed. Storing data files in a cache memory completely defeats their intended purpose. Employing a reference in a manner that defeats its intended purpose is improper, as is explained below in more detail with reference to MPEP §2143.01, entitled "Suggestion or Motivation to Modify the References".

In a subsection entitled "THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE", this MPEP section states that: "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984) ...."

Inasmuch as modifying these teachings to arrive at the subject matter of the claim or attempting to adapt the teachings of Tobita for such renders the teachings the reference unsatisfactory for their intended purpose, there is, as a matter of law, no motivation to modify the teachings of Tobita as suggested by the Office Action. Accordingly, the rejection of claim 33 should be withdrawn, and claim 33 should be allowed.

Independent claim 39 recites "A method comprising: storing volatile data in at least one volatile data file in volatile memory; storing nonvolatile data in at least one nonvolatile data file in nonvolatile memory; receiving a request to access a particular data file; determining whether the particular data file is stored in the volatile memory or the nonvolatile memory; and locating the particular data file", which is not taught, disclosed, suggested or motivated by the cited references, alone or in combination.

The cited portions of Tobita and Chen have been discussed above. The Office Action cites (p. 18) Li (col. 5, lines 47-55) for "storing volatile data in at least one volatile data file in volatile memory; storing nonvolatile data in at least one nonvolatile data file in nonvolatile memory", as recited in claim 39. This

passage is discussed above with reference to claim 28 and fails to provide the subject matter recited in claim 39.

To put the discussion of this passage into the context of claim 39, the system described in Li would not require "determining whether the particular data file is stored in the volatile memory or the nonvolatile memory" in response to "receiving a request to access a particular data file". When such a system receives a request to access a particular data file, that data file is fetched from nonvolatile memory, such as a disc or optical drive.

Accordingly, the rejection of claim 39 is prima facie defective and should be withdrawn, and claim 39 should be allowed.

As well, independent claim 43 recites "A method comprising: storing data produced by a first application within a volatile data file within volatile memory in a smart card; and accessing the volatile data file from a second application", which is not taught, disclosed, suggested or motivated by the cited references, alone or in combination.

The Office Action cites (p. 20) portions of Tobita addressed above with reference to claim 18 and portions of Li addressed above with reference to claim 39. Nobakht's references to smart cards fail to cure these deficiencies. Accordingly, the rejection of claim 43 is in error and should be withdrawn, and claim 43 should be allowed.

Further, simply providing a conclusory statement that "It would have been obvious ...." fails to meet the standards set forth in the MPEP for establishing a prima facie case of unpatentability. These are set forth in MPEP §2143, entitled

"Basic Requirements of a Prima Facie Case of Obviousness" (see also MPEP §706.02(j), §2141 et seq. and §2142).

This MPEP section states that "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." The references fail to teach or disclose the elements recited in the claims. Accordingly, the references cannot provide motivation to modify their teachings to arrive at the invention as claimed, and the Examiner has identified no such teaching or disclosure in the references. As a result, the first prong of the test cannot be met.

MPEP §2143 further states that "Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

Inasmuch as the references fail to provide all of the features recited in Applicant's claims, the third prong of the test is not met. As a result, there cannot be a reasonable expectation of success. As such, the second prong of the test cannot be met.

MPEP §2143 additionally states that "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." This fourth criterion cannot be met because the references fail to teach or disclose the elements recited in the claim. As such, the

unpatentability rejections fail all of the criteria for establishing a prima facie case of obviousness as set forth in the MPEP.

Moreover, no evidence has been provided as to why it would be obvious to combine or modify the teachings of these references. Evidence of a suggestion to combine or modify may flow from the prior art references themselves, from the knowledge of one skilled in the art, or from the nature of the problem to be solved. However, this range of sources does not diminish the requirement for actual evidence. Further, the showing must be clear and particular. See *In re Dembiczak*, 175 F.3d 994, 998 (Fed. Cir. 1999).

Dependent claims 2-9, 11-17, 19, 21-24, 26, 27, 30-32, 34-38, 40-42, 44 and 45 (as filed) distinguish for their own recited features and by virtue of dependence from allowable claims. Accordingly, the unpatentability rejection of claims 2-6 and 8-45 is defective and should be withdrawn, and claims 2-6 and 8-45 should be allowed.

Conclusion

Claims 1-6 and 8-53 are in condition for allowance. Applicant respectfully requests reconsideration and issuance of the subject application. Should any matter in this case remain unresolved, the undersigned attorney respectfully requests a telephone conference with the Examiner to resolve any such outstanding matter.

Respectfully Submitted,

Date: Dec. 23, 2005

By: _____

Frederick M. Fliegel
Reg. No. 36,138
(509) 324-9256 x239

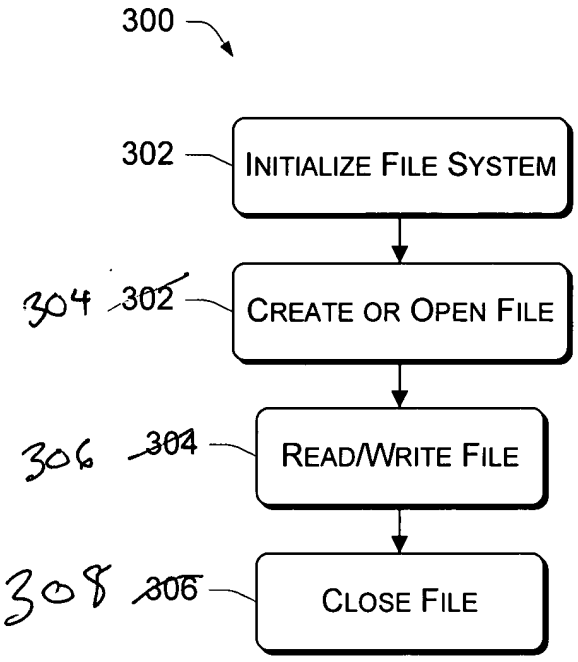

Fig. 3